## REMARKS

Claims 1 – 30 remain in the application and stand finally rejected. The final rejection is respectfully traversed.

Curiously, the specification is objected to for containing informalities on page 9, lines 13 and 16. Applicants note that, page 9, line 5 – page 10, line 2 was amended in the previous response, with the serial numbers included in an amendment provided for page 1 as well. Thus, no further amendment is believed needed. Reconsideration and withdrawal of the objection to the specification is respectfully solicited.

Claims 1 – 30 are rejected under 35 U.S.C. §§102(b) and 103(a) over E.P. 125,733 to Feller. Specifically, it is alleged that "Feller clearly discloses a first buffer/inverter (10; see page 7, lines 16+), a second buffer/inverter (20), and a supply select/threshold drop element (30)." The rejection is respectfully traversed.

Applicants note that for the first time, claims 11, 17 and 29 are substantively rejected in this final rejection. In the prior Office action, claims 11, 17 and 29, were only rejected under 35 U.S.C. §112. Thus, clearly, the applicants successfully overcame the prior rejection, which is not repeated in this final Office action. The lack of any substantive rejection was specifically noted in the applicants response to that prior Office action. Furthermore, MPEP §706.07(a) provides that "second or any subsequent actions **on the merits** shall be final," which is not the case for claims 11, 17 and 29. Therefore, the applicants respectfully request withdrawal of the finality of the rejection as being improper with respect to claims 11, 17 and 29.

Regarding newly rejected claim 17, it is asserted that "'the FET is a high threshold voltage FET' **does not mean much** because it can be interpreted that any FET has a high threshold voltage compared to any other FET having lower threshold voltage."

As far as the applicants are aware, this is not the standard for patentability under 35 U.S.C. §102(b). "A claim is anticipated only if each and every element as set forth in the claim is **found**, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention **must be shown** in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). MPEP 2131. Thus, an assertion that a recitation in a claim "**does not mean much**" has no bearing on whether "[t]he identical invention **must be shown** in as complete detail as is contained in the ... claim."

Moreover, an assertion that "it can be interpreted that any FET has a high threshold voltage compared to any other FET having lower threshold voltage," still does not assert that the reference teaches the invention as recited; merely that it could be modified to teach it. Furthermore, there is nothing in Feller to provide any basis to infer or suggest that either the NFET (N4) or PFET (P4) in the allegedly equivalent Feller "supply select/threshold drop element (30)" is any different than the other Feller NFETs N1 – N3 or PFETs P1 – P3. Accordingly, Feller fails to teach "each and every element as set forth in the claim" (17) and so, does not teach the present invention "in as complete detail as is contained in ... claim" 17. *Supra*. Therefore, Feller does not anticipate newly rejected claim 17. Reconsideration and withdrawal of the final rejection of newly rejected claim 17 under 35 U.S.C. §102(b) over Feller is respectfully requested.

Furthermore, regarding the rejection of claims 1 – 5, 7 – 10, 12 – 15, 18 – 23, 25 – 28 and 30, applicants previously noted that Feller neither teaches nor suggests that "standby power is substantially eliminated" in the level converter when the input/output is high as claims 1 and 12 recite. This was addressed in the Office action with regard to

claims 1 and 12: the "TTL circuit not only receives 2.0 volts but also receives voltage up to 5.0 volts. Therefore, **assuming** 3.0V is an input voltage, Vsg=3.6V - 3.0V = 0.6V which is less than 1.4V." (emphasis added). This assumption is not supported with any specific cite anywhere in Feller. Nor could it be.

Feller very clearly teaches CMOS circuits that are compatible with TTL logic signal inputs. See, e.g., Feller Abstract, lines 1 – 3. While Feller does discuss circuit switching characteristics over the range "from $V_{SS}$ to $V_{DD}$," this certainly is not he same as teaching operating at a 3.0V input voltage as the Office action suggests and which is necessary to support a finding of anticipation under 35 U.S.C. §102(b). Further, operating the Feller circuit with input swings "from $V_{SS}$ to $V_{DD}$" operates the Feller circuit as a just another CMOS to CMOS circuit and frustrates the purpose of Feller. Certainly teaching operating the Feller circuit with input swings "from $V_{SS}$ to $V_{DD}$" does not teach a "level converter for interfacing circuits supplied by different supply voltages," as claim 1 recites, and with similar recitations in claim 12. Therefore, Feller neither teaches nor suggests that, "standby power is substantially eliminated" in the Feller level converter as claims 1 and 12 recite. Reconsideration and withdrawal of the rejection of claims 1 and 12 under 35 U.S.C. §102(b) over Feller is respectfully requested.

Likewise, applicants previously noted that Feller neither teaches nor suggests an IC high and low voltage circuits being interfaced by a level converter as recited by Claim 19. This addressed in the Office action by asserting that "it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987)." No such prior art apparatus (IC) has been made of record. Apparently, instead this is directed to including a preferred level converter on an IC, not to the IC itself. While this may be a basis for an obviousness rejection, it is insufficient to support *prima facie* anticipation of the claimed IC, which requires that "each and every element as set forth in the claim is **found**, either

expressly or inherently described, in a single prior art reference." *Supra*. Thus, as neither the IC, the high voltage circuits, nor the low voltage circuits are found in Feller, the present invention as recited in claim 19 is not anticipated by Feller.

Further, should this assertion be treated, instead, as an obvious rejection over Feller in combination with "what is well known in the art," i.e., Official Notice; MPEP 2144.03 provides in pertinent part

> C. If Applicant Challenges a Factual Assertion as Not Properly Officially Noticed or not Properly Based Upon Common Knowledge, the Examiner Must Support the Finding With Adequate Evidence
> To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art. ... If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained."
> E. Summary
> Any rejection based on assertions that a fact is well-known or is common knowledge in the art without documentary evidence to support the examiner's conclusion should be judiciously applied. Furthermore, as noted by the court in *Ahlert*, any facts so noticed should be of notorious character and serve only to "fill in the gaps" in an insubstantial manner which might exist in the evidentiary showing made by the examiner to support a particular ground for rejection. It is **never appropriate** to rely **solely** on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based. See *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697; *Ahlert*, 424 F.2d at 1092, 165 USPQ 421.

(ellipsis original, emphasis added). The substance of such an assertion of obviousness is that including Feller in an Integrated Circuit (IC) to interface TTL IC circuits with CMOS IC circuits is nothing new.

Feller neither shows nor suggests TTL circuits on a CMOS chip or vice versa. Neither are the applicants aware of, nor is there anything of record to teach or suggest, such a combination of incompatible technologies on a single chip. However, for the

combination of Feller with what is well known to result in the present invention as recited in claim 19, just such a combination of CMOS and TTL on a single IC must be well known and suggested. Accordingly, because such a combination of incompatible technologies on a single chip, Feller does not teach or suggest the present invention as recited in claim 19. Reconsideration and withdrawal of the rejection of claim 19 under 35 U.S.C. §102(b) over Feller is respectfully requested.

Regarding newly rejected claims 11 and 29, it is asserted that "'it is well known in the art that the NFET of a CMOS inverter having high threshold voltage reduces leakage current. Therefore, it would have been obvious at the time the invention was made to an ordinary skilled in the art to have provided NFET of Feller with higher threshold voltage in order to reduce leakage current." Where is this supported in Feller? It is not. Where is this suggested in Feller? Again it is not. The applicants cannot help but wonder, if this is such an obvious modification of the Feller CMOS circuit, why didn't Feller think of it. Clearly, it is not. Instead, it is apparent that the application is being used in hindsight for the suggestion. Such a use of the application, in hindsight to suggest modification is improper. Therefore, because the present application is being used in hindsight for a suggestion to modify Feller to result in the present invention as recited in newly rejected claims 11 and 29, claims 11 and 29 are not obvious in view of Feller in combination with what is well known. Reconsideration and withdrawal of the rejection of claim 11 and 29 under 35 U.S.C. §103(a) over Feller is respectfully requested.

Furthermore, because dependent claims include all of the differences with the prior art as the claims from which they depend, Feller does not teach or suggest the present invention as recited in any of claims 2 – 5, 7 – 10, 13 – 15, 18, 20 – 23, 25 – 28 and 30, which depend from claims 1, 12, and 19. Reconsideration and withdrawal of the rejection of claims 2 – 5, 7 – 10, 13 – 15, 18, 20 – 23, 25 – 28 and 30 under 35 U.S.C. §102(b) and claims 6, 16 and 24 under 35 U.S.C. §103(a) over Feller is respectfully requested.

The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance for the reasons set forth above, the applicants respectfully request that the Examiner, reconsider and withdraw finality of the rejection, reconsider and withdraw the objection to the specification, reconsider and withdraw the rejection of claims 1 – 30 under 35 U.S.C. §§102(b) and 103(a) and allow the application to issue.

Should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-0510 and advise us accordingly.

Respectfully Submitted,

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(Date)

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